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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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of

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Complete if Known

Application Number	10/015,530
Filing Date	December 12, 2001
First Named Inventor	Robert T. Plunkett
Art Unit	2183
Examiner Name	Aimee Li

Attorney Docket Number	046301/046000 (QST-046 US)
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document Number – Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US 4,380,046	04-12-1983	Fung	
	2.	US 4,758,985	07-19-1988	Carter	
	3.	US 4,870,302	09-26-1989	Freeman	
	4.	US 4,905,231	02-27-1990	Leung et al.	
	5.	US 5,099,418	03-24-1992	Pian et al.	
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	23.	US 6,326,806 B1	12-04-2001	Fallside et al.	
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	38.	US 6,986,142 B1	01-10-2006	Ehlig et al.	

Examiner Signature	Date Considered
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
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				Filing Date	December 12, 2001
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				Art Unit	2183
				Examiner Name	Aimee Li
				Attorney Docket Number	046301/046000 (QST-046 US)

U.S. PUBLISHED PATENT DOCUMENTS

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	39.	US 2002/0133688 A1	09-19-2002	Lee et al.	
	40.	US 2002/0184275 A1	12-05-2002	Dutta et al.	
	41.	US 2003/0074473 A1	04-17-2003	Pham et al.	
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	44.	WO 00/69073	A1	11-16-2000	Wasson		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	45.	Altera Apex 20K 1999	
	46.	Andraka Consulting Group, "Distributed Arithmetic," Obtained from: http://www.fpga-guru.com/distribu.htm (1998-2000)	
	47.	Hanna et al., "A Normalized Backpropagation Learning Algorithm for Multilayer Feed-Forward Neural Adaptive Filters," <i>Neural Networks for Signal Processing XI</i> , Proceedings of the 2001 IEEE Signal Processing Society Workshop pp. 63–72 (Sept 2001)	
	48.	Janweijer et al., "A Compact Robin Using the SHarc (CRUSH)," Obtained from: http://www.nikhef.nl/~peterj/Crush/CRUSH-hw.pdf (Sept 1998)	
	49.	Rajagopalan et al., "A Flexible Multiplication Unit for an FPGA Logic Block," <i>Circuits and Systems</i> 4:546–9 (2001)	
	50.	Xilinx Data Book 1998	
	51.	Xilinx Virtex 1.1 1998	
	52.	Xilinx Virtex 2.2 2000	

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